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PATENT ABSTRACTS OF JAPAN

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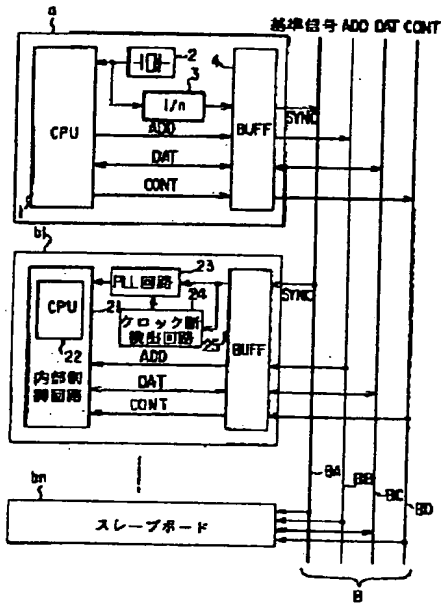
(54) PROCESSOR SYSTEM

(57) Abstract:

PURPOSE: To provide the processor system which can increase the operation speed of each board without causing trouble such as crosstalk, skew between signals, etc.

CONSTITUTION: A frequency divider 3 of a master board (a) divides the frequency of a master clock into a frequency lower than the maximum propagation frequency of a system bus B, and distributes the frequency-divided clock signal to respective slave boards b1-bn as a reference signal through a reference signal line BA, and the slave boards b1-bn generate internal operation clocks in subordinate synchronism with the reference signal by PLL circuits 23 and supply them to internal control circuits 21.



* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] In the processor system which connects two or more boards containing at least one processor board through a common system bus The master board which serves as a clock master among two or more aforementioned boards A dividing means to carry out dividing of the master clock generated by master clock occurrence means to generate a master clock, and this master clock occurrence means to a frequency lower than the maximum propagation frequency decided by the transmission characteristic of the aforementioned system bus, and to generate a reference signal, Have a reference-signal sending-out means to send out the reference signal generated by this dividing means to the aforementioned system bus, and among two or more aforementioned boards boards other than the aforementioned master board The processor system characterized by having a subordinate clock generation means to have PLL circuit which generates the subordinate clock which consists of a necessary frequency which carried out slave synchronization to this reference signal, based on the reference signal sent from the aforementioned master board through the aforementioned system bus.
[Claim 2] A subordinate clock generation means is a processor system according to claim 1 characterized by having a signal monitoring means to supervise the existence of the reference signal which comes through a system bus, and PLL circuit which serves as the self-propelled mode at this reference-signal ******, and continues an occurrence operation of the aforementioned subordinate clock when ** of a reference signal is detected by the aforementioned signal monitoring means during occurrence of a subordinate clock.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] this invention relates to the system which connected two or more boards which contain at least one processor board especially through the common system bus with respect to the processor system used with large-scale data-processing machines, such as a packet switch.
[0002]
[Description of the Prior Art] In the comparatively large-scale data processor, many ********** systems which connected two or more boards which contain a processor board as central-process section through the common system bus are used. Drawing 2 - view 5 shows the structure of a system known conventionally.
[0003] The system first shown in drawing 2 generates the clock which became independent in each board unit, and operates. That is, it connects with system bus B-2, and each board a20 - a2n have the clock generator 201, respectively. Each board a20 - a2n operate with the clock uniquely generated from these clock generators 201, respectively.
[0004] The system shown in drawing 3 on the other hand distributes a clock to each of other slave board through a system bus from one clock master board. That is, the clock signal generated from the clock generator 301 prepared in the master board a3 is distributed to each slave board b31 - b3n through a system bus B3, and each slave board b31 - b3n operate with the distributed clock.
[0005] Moreover, the system shown in drawing 4 distributes a clock to each of other slave board b41 - b4n in the shape of a daisy chain through a system bus B4 from one master board a4.
[0006] The system furthermore shown in drawing 5 inverts the clock which came from the board by the side of the upstream in each slave board b51 - b5n, and transmits it to the board by the side of a lower stream of a river while it distributes a clock to each of other slave board b51 - b5n in the shape of a daisy chain through system bus B5 from one master board a5.
[0007]
[Problem(s) to be Solved by the Invention] There were the following technical probrems which should be solved in these conventional systems. In the system first shown in drawing 2 , in order for various kinds of skews between signals, a contention tone constant skew, etc. in system bus B-2 to arise, it is necessary to make transmission speed as a bus cycle into a low speed. Moreover, the data acknowledgement between each board and problems, such as becoming late one period rather than the retardation expected, since it had answered while it had been asynchronous, are produced.
[0008] On the other hand, since a clock is distributed to each slave board by the bus connection from a master board in the system shown in drawing 3 , compared with the system of above-mentioned view 2 , improvement in the speed of a clock is possible. However, since it has connected to a system bus with each board using TTL interface, about at most 20MHz becomes a limitation, and, as for a clock rate, the improvement in the speed beyond it is impossible. Moreover, when it is going to distribute a clock independently of each board, the cross talk noise on a system bus increases, and the failure not to consider occurs, or there is fault which clock skew generates.
[0009] Moreover, in some which connect each slave board in the shape of a daisy chain to a master board like the system shown in the drawing 4 and the drawing 5 , the signal retardation by the gate for daisy chains of each slave board is large, and there is a problem to which the speed of a system bus will be restricted for this reason. Moreover, occurrence of clock skew could not be prevented but

there was fault of the grade by which a slot package is restrained further.
[0010] It aims at offering the ********** system which can realize improvement in the speed of the working speed of each board, without making this invention in view of the above situations, and producing faults, such as a cross talk and a skew between signals.
[0011]
[Means for Solving the Problem] In the processor system which connects two or more boards on which this invention contains at least one processor board through a common system bus A master clock occurrence means to generate a master clock on the master board which serves as a clock master among two or more aforementioned boards, A dividing means to carry out dividing of the master clock generated by this master clock occurrence means to a frequency lower than the maximum propagation frequency decided by the transmission characteristic of the aforementioned system bus, and to generate a reference signal, It has a reference-signal sending-out means to send out the reference signal generated by this dividing means to the aforementioned system bus. And it is based on the reference signal sent to boards other than the aforementioned master board from the aforementioned master board through the aforementioned system bus among two or more aforementioned boards. It has a subordinate clock generation means to have PLL circuit which generates the subordinate clock which consists of a necessary frequency which carried out slave synchronization to this reference signal.
[0012] Moreover, this invention is characterized also by setting PLL circuit as the self-propelled mode at this reference-signal ******, and continuing an occurrence operation of the aforementioned subordinate clock, when it has a signal monitoring means to supervise the existence of the reference signal which arrives at the subordinate clock generation means mentioned above through a system bus and ** of a reference signal is detected by the aforementioned signal monitoring means during occurrence of a subordinate clock.
[0013]
[Function] Consequently, since the clock by which dividing was carried out to below the maximum propagation frequency of a system bus with the counting-down circuit to the slave board will be sent as a reference signal from the master board used as a clock master according to this invention, occurrence of the cross talk on a system bus etc. is prevented. Moreover, in the aforementioned slave board, the clock of the slave synchronization necessary-to this reference signal frequency on the basis of the reference signal sent from the aforementioned master board is generated by clock generation means to have PLL circuit, and this subordinate clock is used as a clock of the aforementioned slave board of operation by it. For this reason, it will operate, after the aforementioned slave board has synchronized with the aforementioned master board completely, and thereby, occurrence of the dead times at the skew between signals, the time of bus contention, etc. is suppressed to the minimum extent. moreover, since it is possible to generate the high-speed clock needed on the aforementioned slave board, a fast turn around is possible for the aforementioned slave board -- ** -- ** That is, the system which realized both enhancement in a stability and improvement in the speed of a working speed can be offered.
[0014] Moreover, if according to this invention the existence of arrival of a reference signal is supervised in a slave board and arrival of a reference signal serves as ** during subordinate clock generation, the aforementioned slave board will serve as the self-propelled mode, and occurrence of a subordinate clock will be continued. For this reason, even if a reference clock serves as ** temporarily for a certain ground, the aforementioned slave board becomes possible [continuing an operation], without the being influenced directly, and, thereby, can raise the stability of a system further.
[0015]
[Example] Drawing 1 is a circuit block diagram showing the ********** structure of a system concerning one example of this invention. In this drawing, the master board on which a serves as a clock master, and b1-bn show the slave board, and B shows the system bus, respectively. System bus B consists of reference-signal line BA, address bus BB, a data bus BC, and a control bus BD.
[0016] Master board a has CPU1 which performs a main control of a system, and has the clock generator 2, the counting-down circuit 3, and the buffer 4 further. A clock generator 2 generates a high-speed master clock signal required for an operation of CPU1, and supplies this master clock to

CPU1. A counting-down circuit 3 carries out dividing of the above-mentioned master clock signal to 1/n (n= 1, 2, --), and, thereby, generates a reference signal. Here, rather than the maximum propagation frequency (the highest cut off frequency) decided with propagation properties, such as the distributed capacity of system bus B, and a capacitive load, n is set up so that a reference-signal frequency may become low. The reference signal outputted from the above-mentioned counting-down circuit 3 is delivered through a buffer 4 to the reference-signal line BA.

[0017] In addition, address ADD, the data DAT, and control signal CONT which were outputted from CPU1 are delivered through a buffer 4 to address bus BB, the data bus BC, and the control bus BD of system bus B, respectively.

[0018] On the other hand, the slave boards b1-bn have the internal-control circuit 21 equipped with CPU22, and have the buffer 25 which performs buffering of address ADD, data DAT, and control signal CONT further between this internal-control circuit 21 and each buses BB, BC, and BD of the above-mentioned system bus B, the PLL circuit 23, and the clock-stop detector 24.

[0019] On the basis of the reference signal inputted through the buffer 25 from the reference-signal line BA, the PLL circuit 23 generates the interior-action clock of the frequency which synchronizes with this reference signal and is needed in CPU22, and supplies this clock to the internal-control circuit 21. The clock-stop detector 24 has the function to detect disappearance of the reference signal which comes through system bus B. The PLL circuit 23 serves as the self-propelled mode in the term when disappearance of a reference signal is detected in the above-mentioned clock-stop detector 24.

[0020] Next, an operation of the system constituted as mentioned above is explained. In the clock generator 2 in master board a, a master clock is generated and this master clock is supplied to CPU1 as a clock of operation. Moreover, after 1/n (n= 1, 2, --) dividing of the above-mentioned master clock is carried out in a counting-down circuit 3 and it serves as a low frequency from the maximum propagation frequency of system bus B by this, it is outputted to the reference-signal line BA of system-buffer B through a buffer 4, and is sent to each slave boards b1-bn through this reference-signal line BA.

[0021] That is, on the reference-signal line BA, the clock with which the frequency was low stopped rather than the maximum propagation frequency of system bus B will be transmitted. For this reason, faults, such as a cross talk, are not produced on system bus B.

[0022] On the other hand, with each slave boards b1-bn, on the basis of the reference signal which came through the above-mentioned reference-signal line BA, it synchronizes with the reference signal of a PLL circuit 23 smell lever, and a high-speed interior-action clock required for an operation of CPU22 is generated. And this interior-action clock is supplied to CPU22.

[0023] Therefore, slave synchronization of each slave boards b1-bn will be completely carried out to both reference signals, and it will operate synchronizing with a high-speed clock required for an operation of CPU22. For this reason, a high-speed operation is attained with each slave boards b1-bn, without producing the skew between signals etc.

[0024] Moreover, suppose that the reference signal disappeared temporarily according to a certain cause under above-mentioned operation. If it does so, disappearance of this reference signal will be detected by the clock-stop detector 24, and the PLL circuit 23 will become the self-propelled mode during the disappearance of this reference signal. For this reason, from the PLL circuit 23, an interior-action clock is generated succeedingly. Therefore, the internal-control circuit 21 containing CPU22 can continue a processing operation according to this clock.

[0025] Thus, according to this example, in the counting-down circuit 3 of master board a, dividing of the master clock is carried out to a frequency lower than the maximum propagation frequency of system bus B. It distributes to each slave boards b1-bn through the reference-signal line BA, using as a reference signal this clock signal by which dividing was carried out. And since the interior-action clock which carried out slave synchronization to the above-mentioned reference signal in the PLL circuit 23 with the slave boards b1-bn is generated and it was made to supply the internal-control circuit 21 Altogether, each slave boards b1-bn can synchronize with master board a completely, and can operate, and the full synchronization of system bus B of them is attained. For this reason, the dead times at the skew between signals, the time of bus contention, etc. can be stopped to the minimum extent. Moreover, since the clock frequency on system bus B of a reference signal is set below to the maximum propagation frequency, the fault which a cross talk noise etc. generates on

system bus B is also lost. Therefore, each board can offer the stable system in which a fast turn around is possible.
[0026] Moreover, according to this example, even if a reference signal disappears temporarily, this is detected by the clock-stop detector 24, the PLL circuit 23 serves as the self-propelled mode, and thereby, an interior-action clock continues and is generated. For this reason, the interior action in the slave boards b1-bn is guaranteed, and, thereby, can raise the stability of a system of operation further. In addition, this invention is not limited only to the above-mentioned example, but in the domain which does not change a summary, deforms suitably and can be carried out.
[0027]
[Effect of the Invention] In the master board on which this invention serves as a clock master among two or more boards Carry out dividing of the master clock to a frequency lower than the maximum propagation frequency decided by the transmission characteristic of a system bus, and a reference signal is generated. Deliver this generated reference signal to a system bus, and it sets on boards other than the aforementioned master board among two or more aforementioned boards. Based on the reference signal sent from the aforementioned master board through the aforementioned system bus, it is made to generate the subordinate clock which consists of a necessary frequency which carried out slave synchronization to this reference signal.
[0028] Therefore, the processor system which realized both enhancement in a stability and improvement in the speed of a working speed can be offered, and the stability and rapidity of operations, such as equipment, which are equipped with the concerned processor system by this can be promoted.
[0029] Moreover, according to this invention, in occurrence of the subordinate clock mentioned above, the existence of the reference signal which comes through a system bus is supervised. Since the occurrence operation of the aforementioned subordinate clock was continued, using PLL circuit as the self-propelled mode at this reference-signal ****** when ** of a reference signal was detected during occurrence of the aforementioned subordinate clock The stability of a processor system can be raised further and the stability of operations, such as the equipment equipped with the concerned processor system by this, can be promoted.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The block diagram showing the configuration of the central-process section of the data processor in one example of this invention.
[Drawing 2] The block diagram showing the configuration of the conventional central-process section.
[Drawing 3] The block diagram showing the configuration of the conventional central-process section.
[Drawing 4] The block diagram showing the configuration of the conventional central-process section.
[Drawing 5] The block diagram showing the configuration of the conventional central-process section.
[Description of Notations]
a-- master board, and b1 - bn-- a slave board, B-- system bus, BA-- reference-signal line, and BB-- an address bus, BC-- data bus, BD-- control bus, and 1 -- CPU, 2 -- clock generator, 3 -- counting-down circuit, and 4 -- a buffer, 21 -- internal-control circuit, 22 --CPU, and 23 -- PLL circuit, 24 -- clock-stop detector, and 25 -- buffer

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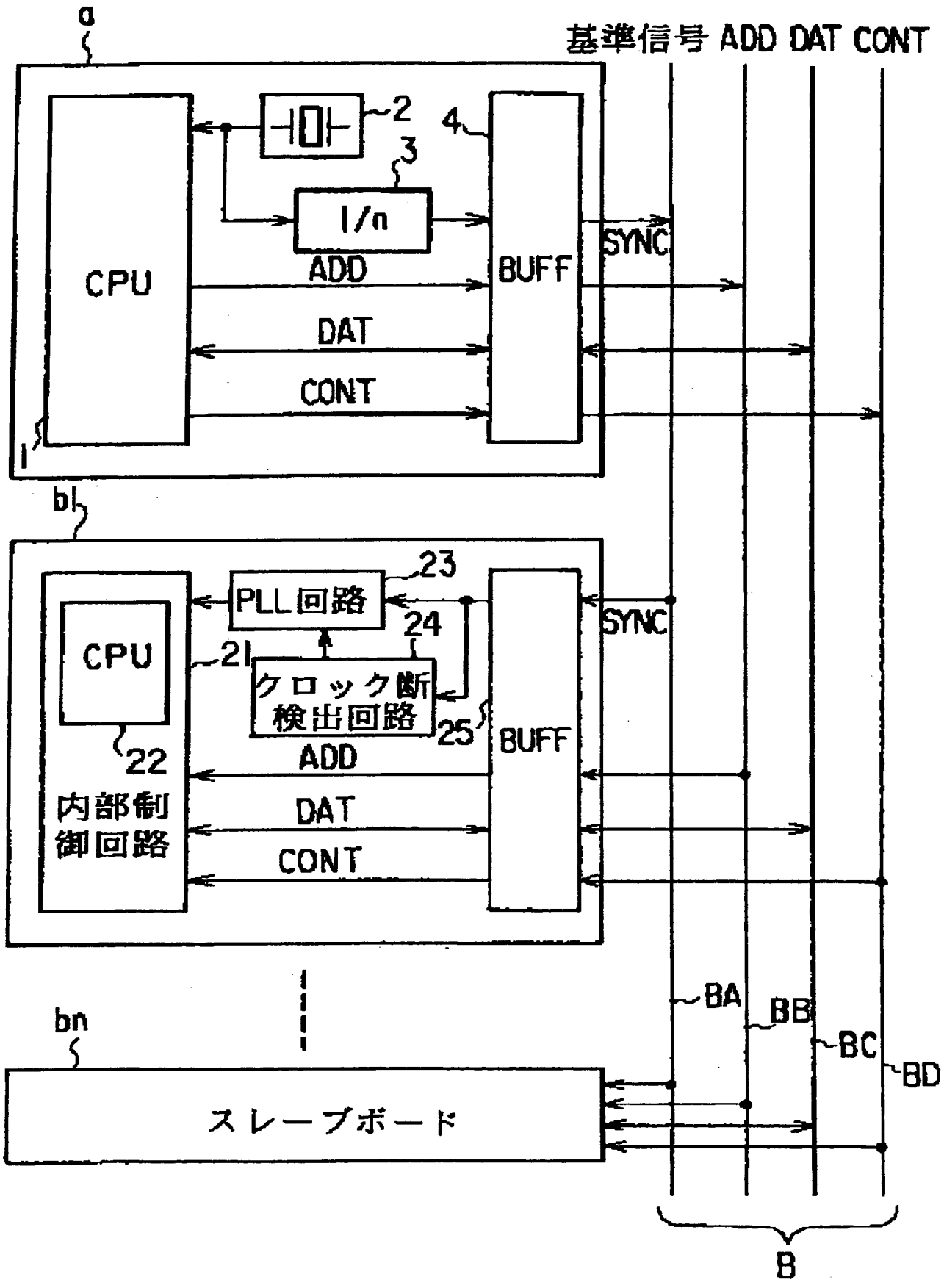
[Translation done.]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CPU
2
3
4
1/n
ADD
DAT
CONT
BUFF
SYNC
1
b1
PLL回路
23
24
CPU
21
クロック断
検出回路
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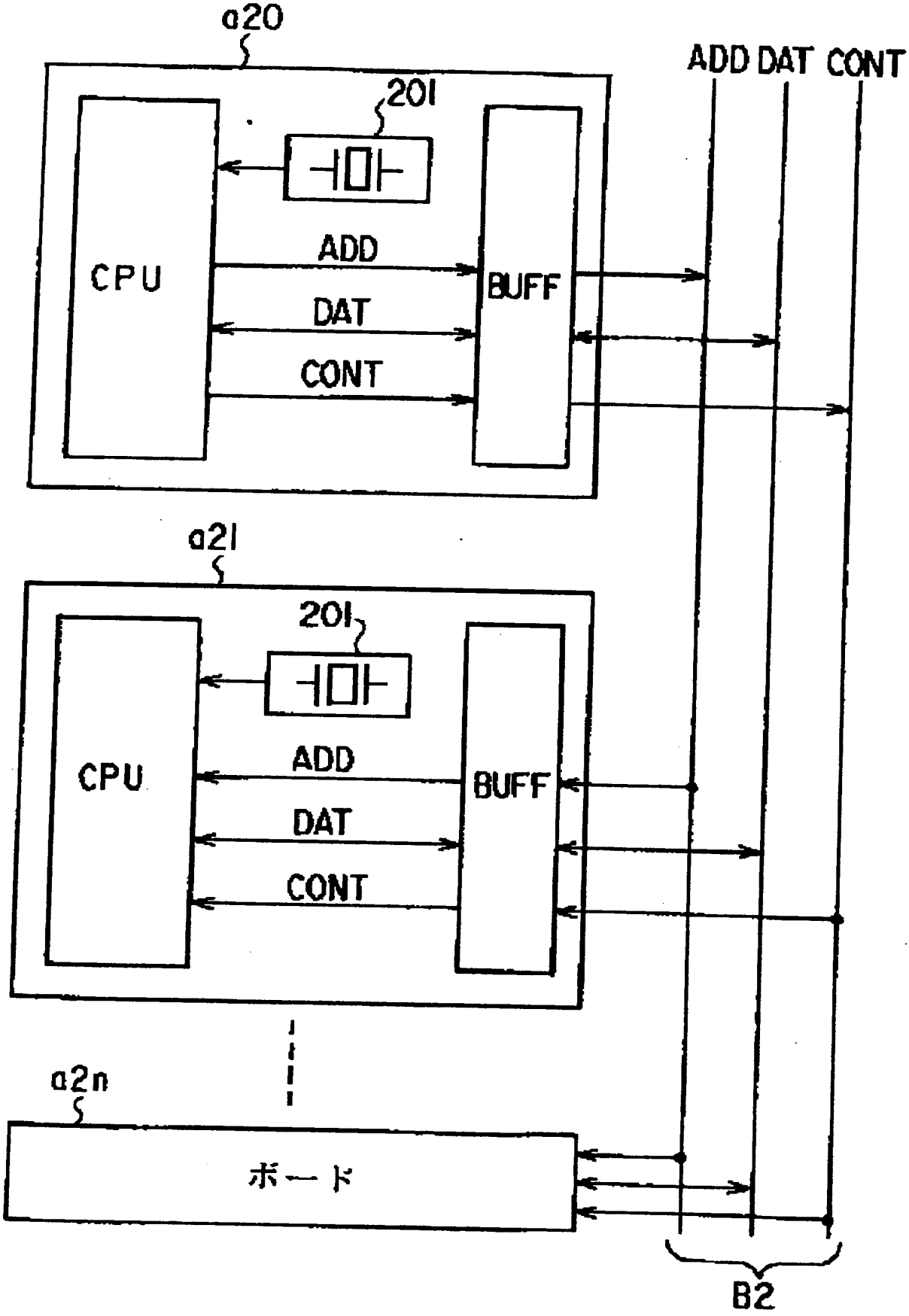
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ADD DAT CONT
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CPU
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CONT
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a2n
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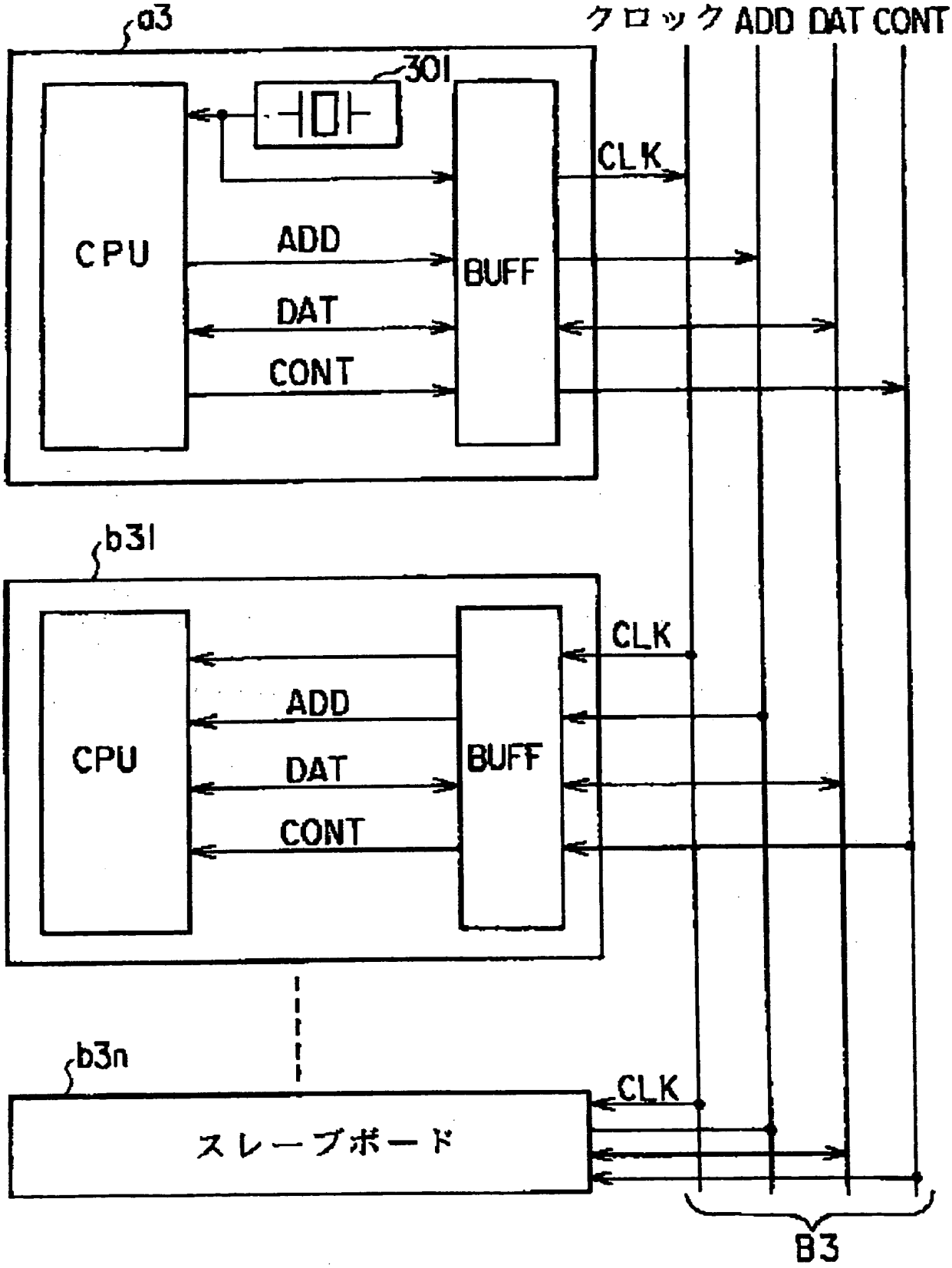
B2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CLK
ADD
DAT
CONT
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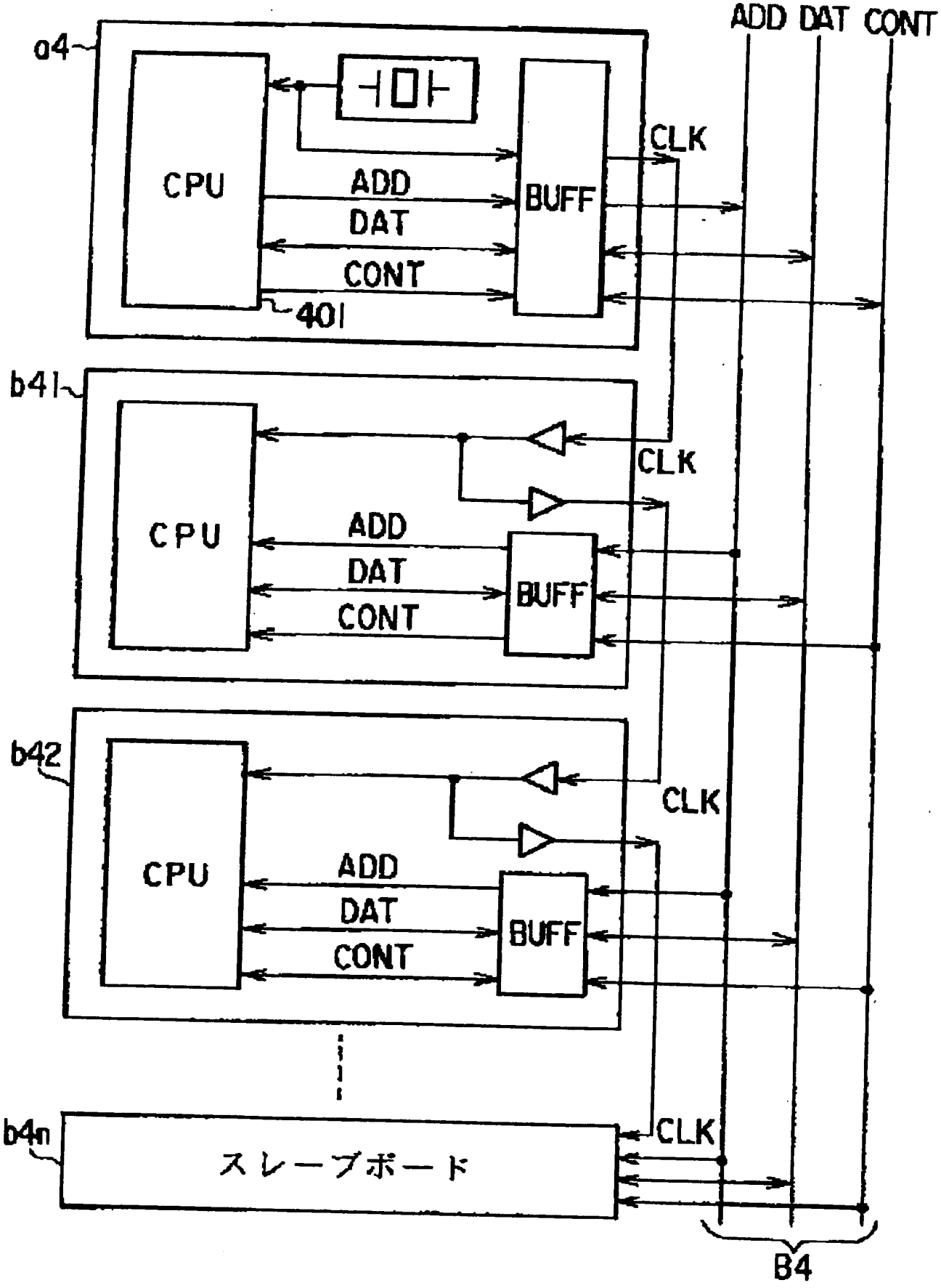
スレーブボード
B3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ADD
DAT
CONT
CLK
b41
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BUFF
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BUFF
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CLK
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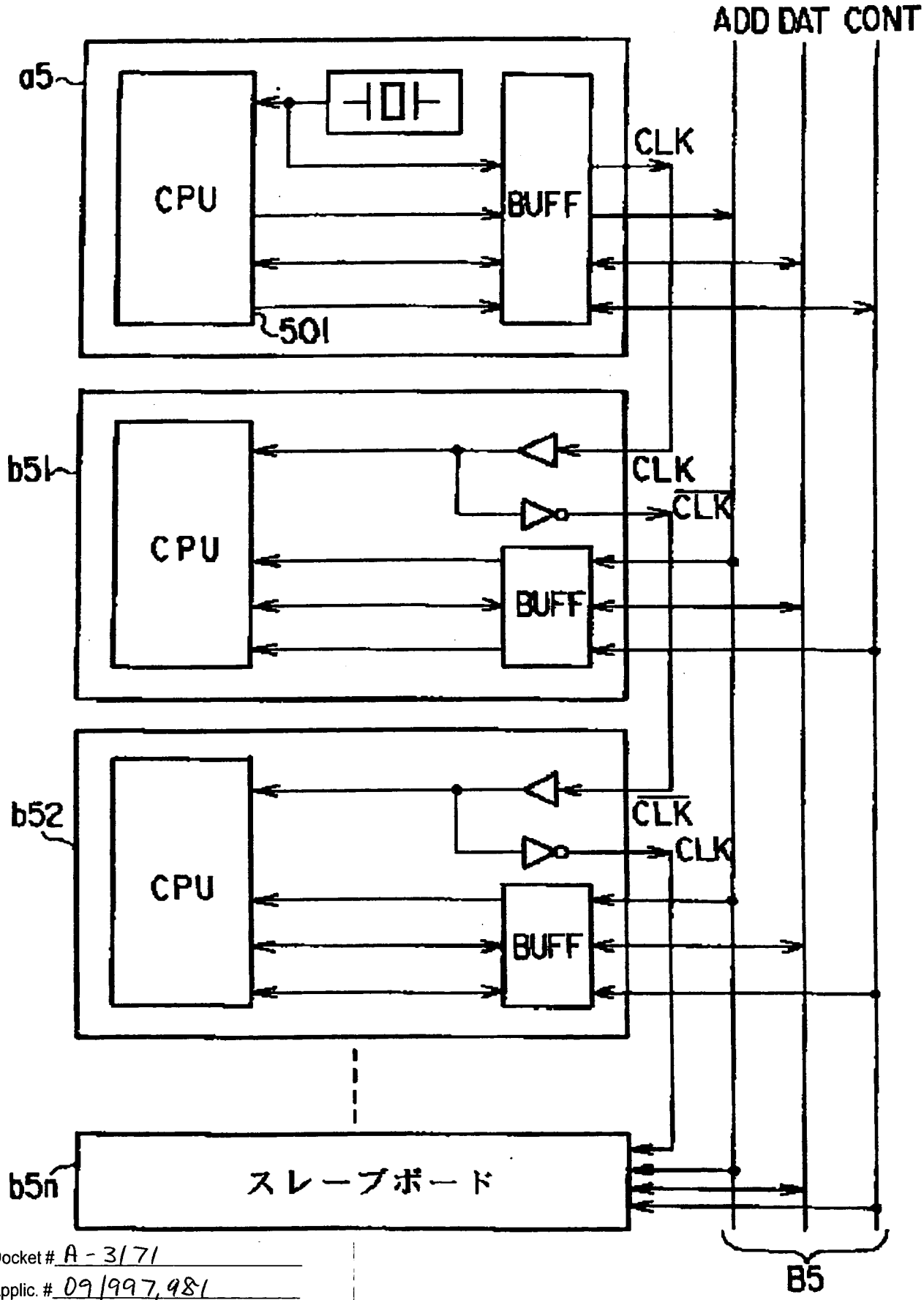
スレーブボード
CLK
B4



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